1. In a system that includes a master component that is configured to communicate with one or more slave components over a clock wire and a data wire, a method for the master component reliably communicating with the one or more slave components using a guaranteed header two-wire interface, the method comprising the following:

an act of determining that a read operation is to be performed on a slave component of the one or more slave components;

an act of transmitting at least a portion of a frame to the one or more slave components using the data wire, the portion of the frame identifying the read operation;

an act of transferring control of the data wire to the slave component;

an act of receiving reliability data from the slave component over the data wire; and

an act of using the reliability data to determine if there is a problem with the read operation being performed on the slave component.

2. A method in accordance with Claim 1, wherein the reliability data is cyclic redundancy checking data generated by the slave component, the method further comprising the following:

an act of the generating cyclic redundancy checking data at the master component as well, wherein the act of using the reliability data to determine if there is a problem with the read operation being performed on the slave component comprises an act of comparing the cyclic redundancy checking data generated by the master component with the cyclic redundancy checking data generated by the slave component.

3. A method in accordance with Claim 2, further comprising the following:

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an act of determining that the cyclic redundancy checking data generated by the master component matches the cyclic redundancy checking data generated by the slave component.

4. A method in accordance with Claim 2, further comprising the following:

an act of determining that the cyclic redundancy checking data generated by the master component does not match the cyclic redundancy checking data generated by the slave component.

5. A method in accordance with Claim 4, further comprising the following:

an act of reinitiating transmission of the frame upon determining that the cyclic redundancy checking data does not match.

6. A method in accordance with Claim 1, wherein the reliability data comprises an acknowledgement generated by the slave component.

7. A method in accordance with Claim 1, wherein the acknowledgement is a Boolean value in which one binary value indicates a successful acknowledgement and the opposite binary value indicates an unsuccessful acknowledgement.

8. A method in accordance with Claim 1, wherein the act of using the reliability data to determine if there is a problem with the read operation being performed on the slave component comprises the following:

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an act of determining from the acknowledgement that the read operation was successful.

9. A method in accordance with Claim 1, wherein the act of using the reliability data to determine if there is a problem with the read operation being performed on the slave component comprises the following:

an act of determining from the acknowledgement that the read operation was not successful.

10. A method in accordance with Claim 1, further comprising the following:

an act of reinitiating transmission of the frame upon determining that the read operation was not successful.

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11. In a system that includes a master component that is configured to communicate with one or more slave components over a clock wire and a data wire, a method for the slave component reliably communicating with the master component using a guaranteed header two-wire interface, the method comprising the following:

an act of receiving over the data wire at least a portion of a frame from the master component, the portion of the frame indication that a read operation is to be performed on the slave component;

an act of receiving control of the data wire from the master component;

an act of transmitting reliability data to the master component over the data wire.

12. A method in accordance with Claim 11, wherein the reliability data is cyclic redundancy checking data generated by the slave component, the method further comprising the following:

an act of the generating the cyclic redundancy checking data at the slave component.

13. A method in accordance with Claim 11, wherein the reliability data comprises an acknowledgement, the method further comprising the following:

an act of the generating the acknowledgement.

14. A method in accordance with Claim 13, wherein the act of generating the acknowledgement comprises the following:

an act of determining that the read operation was successful; and

in response to determining that the read operation was successful, generating a successful acknowledgement.

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15. A method in accordance with Claim 13, wherein the act of generating the acknowledgement comprises the following:

an act of determining that the read operation was not successful; and

in response to determining that the read operation was successful, generating an unsuccessful acknowledgement.

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16. A system comprising the following:

a master component;

a slave component;

a data wire coupled between the master component and the slave component;

a clock wire coupled between the master component and the slave component;

the master and slave components configured to communicate with each other over the data wire and the clock wire using a guaranteed header two-wire interface, wherein the master component is configured to perform the following:

an act of determining that a read operation is to be performed on the slave component;

an act of transmitting at least a portion of a frame to the one or more slave components using the data wire, the portion of the frame identifying the read operation;

an act of transferring control of the data wire to the slave component;

an act of receiving reliability data from the slave component over the data wire;

an act of using the reliability data to determine if there is a problem with the read operation being performed on the slave component;

wherein the slave component is configured to perform the following:

an act of receiving over the data wire the at least a portion of a frame from the master component;

an act of receiving the control of the data wire from the master component; and

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an act of transmitting the reliability data to the master component over the data wire.

17. A system in accordance with Claim 16, wherein the reliability data is cyclic redundancy checking data generated by the slave component

18. A system in accordance with Claim 16, wherein the reliability data comprises an acknowledgement generated by the slave component.

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19. In a system that includes a master component that is configured to communicate with one or more slave components over a clock wire and a data wire, a method for the master component reliably communicating with the one or more slave components using a guaranteed header two-wire interface, the method comprising the following:

an act of determining that a write operation is to be performed on a slave component of the one or more slave components;

an act of transmitting at least a portion of a frame to the one or more slave components using the data wire, the portion of the frame identifying the write operation;

an act of transferring control of the data wire to the slave component; and

an act of receiving a remaining portion of the frame from the slave component, wherein the frame includes reliability data that indicative of whether or not the operation was successful.

20. A method in accordance with Claim 19, wherein the reliability data is included in at least the portion of the frame and is thus transmitted from the master component to the slave component.

21. A method in accordance with Claim 20, wherein the reliability data comprises cyclic redundancy checking data generated by the master component.

22. A method in accordance with Claim 20, wherein the remaining portion of the frame includes information indicating whether the cyclic redundancy checking data

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generated by the master component matches the cyclic redundancy checking data generated by the slave component.

23. A method in accordance with Claim 19, wherein the reliability data is included in the remaining portion of the frame and is thus transmitted from the slave component to the master component.

24. A method in accordance with Claim 23, wherein the reliability data comprises acknowledgement of success or failure of the write operation.

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25. In a system that includes a master component that is configured to communicate with one or more slave components over a clock wire and a data wire, a method for the slave component reliably communicating with the one or more slave components using a guaranteed header two-wire interface, the method comprising the following:

an act of receiving over the data wire at least a portion of a frame from the master component, the portion of the frame indicating that a write operation is to be performed on the slave component;

an act of receiving control of the data wire from the master component; and

an act of transmitting a remaining portion of the frame from the slave component, wherein the frame includes reliability data that indicative of whether or not the operation was successful.

26. A method in accordance with Claim 25, wherein the reliability data is included in at least the portion of the frame and is thus transmitted from the master component to the slave component.

27. A method in accordance with Claim 26, wherein the reliability data comprises cyclic redundancy checking data generated by the master component.

28. A method in accordance with Claim 26, wherein the remaining portion of the frame includes information indicating whether the cyclic redundancy checking data generated by the master component matches the cyclic redundancy checking data generated by the slave component.

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29. A method in accordance with Claim 28, wherein the reliability data is included in the remaining portion of the frame and is thus transmitted from the slave component to the master component.

30. A method in accordance with Claim 28, wherein the reliability data comprises acknowledgement of success or failure of the write operation.

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31. A system comprising the following:

a master component;

a slave component;

a data wire coupled between the master component and the slave component;

a clock wire coupled between the master component and the slave component;

the master and slave components configured to communicate with each other over the data wire and the clock wire using a guaranteed header two-wire interface, wherein the master component is configured to perform the following:

an act of determining that a write operation is to be performed on a slave component of the one or more slave components;

an act of transmitting at least a portion of a frame to the one or more slave components using the data wire, the portion of the frame identifying the write operation;

an act of transferring control of the data wire to the slave component; and

an act of receiving a remaining portion of the frame from the slave component, wherein the frame includes reliability data that indicative of whether or not the operation was successful; and

wherein the slave component is configured to perform the following:

an act of receiving over the data wire at least the portion of a frame from the master component;

an act of receiving the control of the data wire from the master component; and

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an act of transmitting a remaining portion of the frame from the slave component, wherein the frame includes reliability data that indicative of whether or not the operation was successful.

32. A system in accordance with Claim 31, wherein the reliability data is included in at least the portion of the frame and is thus transmitted from the master component to the slave component.

33. A system in accordance with Claim 32, wherein the reliability data comprises cyclic redundancy checking data generated by the master component.

34. A system in accordance with Claim 32, wherein the remaining portion of the frame includes information indicating whether the cyclic redundancy checking data generated by the master component matches the cyclic redundancy checking data generated by the slave component.

35. A system in accordance with Claim 31, wherein the reliability data is included in the remaining portion of the frame and is thus transmitted from the slave component to the master component.

36. A system in accordance with Claim 35, wherein the reliability data comprises acknowledgement of success or failure of the write operation.

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37. A system in accordance with Claim 31, wherein the system is implemented in a laser transmitter/receiver.

38. A master component in accordance with Claim 38, wherein the laser transmitter/receiver is a 1G laser transceiver.

39. A master component in accordance with Claim 38, wherein the laser transmitter/receiver is a 2G laser transceiver.

40. A master component in accordance with Claim 38, wherein the laser transmitter/receiver is a 4G laser transceiver.

41. A master component in accordance with Claim 38, wherein the laser transmitter/receiver is a 10G laser transceiver.

42. A master component in accordance with Claim 38, wherein the laser transmitter/receiver is a laser transceiver suitable for fiber channels greater than 10G.

43. A master component in accordance with Claim 38, wherein the laser transmitter/receiver is an XFP laser transceiver.

44. A master component in accordance with Claim 38, wherein the laser transmitter/receiver is an SFP laser transceiver.

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45. A master component in accordance with Claim 38, wherein the laser transmitter/receiver is a SFF laser transceiver.

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